

Electronic Filing System (EFS) Data

Electronic Patent Application Submission

USPTO Use Only

EFS ID: 65480
Application ID: 10710699 

Title of Invention: ACCURATE TIMING ANALYSIS OF
INTEGRATED CIRCUITS WHEN
COMBINATORIAL LOGIC OFFERS
A LOAD

First Named Inventor: Somasekar JAYARAMAN

Domestic/Foreign Application: Domestic Application

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U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

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02 FC:1201 86.00 DA

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